In the claims:

1. A method for determining location of a short in a circuit, comprising the steps of :

(a) running a connectivity extract tool on an artwork of the circuit;

(b) determining if a short exists in the circuit, wherein if a short exists the method comprises:

running a short locator tool; and

(c) comparing the artwork of the circuit to a schematic of the circuit.

2. The method of claim 1 wherein the step of running a short locator tool further comprises the steps of:

examining a schematic of the circuit;

creating a copy of the artwork of the circuit; and

inferring labels to the copy of the artwork.

3. The method of claim 2 where in the step of examining further comprises the step of evaluating a connectivity text file of the schematic.

4. The method of claim 3 wherein the step of evaluating further comprises obtaining electrical connection information for each component.

5. The method of claim 2 wherein the step of inferring further comprises the step of renaming signal names.

6. The method of claim 2 further comprising the step of running the connectivity extract tool on the copy of the artwork.

7. The method of claim 6 further comprising obtaining shortest path between conflicting labels in the circuit.

8. The method of claim 7 further comprising modifying artwork of the circuit.

9. The method of claim 8 further comprising running the connectivity extract tool on the modified artwork.

10. A method for determining shortest path for a short in a circuit comprising the steps of:

examining a schematic of the circuit;

creating a copy of the artwork of the circuit; and

inferring labels to the copy of the artwork.

11. The method of claim 10 where in the step of examining further comprises the step of evaluating a connectivity text file of the schematic.

12. The method of claim 11 wherein the step of evaluating further comprises obtaining electrical connection information for each component in the circuit.

13. The method of claim 10 wherein the step of inferring further comprises the step of renaming common connection signal names.

14. The method of claim 10 further comprising the step of running a connectivity extract tool on the copy of the artwork.

15. The method of claim 14 further comprising obtaining shortest path between conflicting labels in the circuit.

16. The method of claim 15 further comprising modifying artwork of the circuit.

17. The method of claim 16 further comprising running the connectivity extract tool on the modified artwork.